



Design and Implementation of Optimized Reversible 9's and 10's Complement Code Converter for Applications in Quantum Computing

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Abstract

In this article, the authors proposed the new cost-optimized reversible 9's and 10's complement code converter for applications in quantum computations using basic reversible gates. The proposed 9's complement code converter uses one Peres gate (PG) and four reversible NOT gates. The quantum cost (QC), garbage output (GO), constant input (CI), and Delay are 8, 0, 0, and 3 respectively. The new reversible 10's complement code converter uses two PG, one Feynman gate (FG), and three NOT gates. The QC, GO, CI, and Delay of the proposed 10's complement code converter circuit are 12, 1, 1, and 4 respectively. The parameters of the proposed 9's complement are improved significantly. The improvement of QC, GO, CI, and Delay is 61.9% – 73.3%, 100%, 100%, and 40% – 50% respectively w.r.t. previously reported results. The proposed circuit has been implemented and verified using the Qiskit by the IBM Quantum Computing lab. The proposed circuits are identical in quantum information processing, cryptography, etc.

Keywords: Quantum computing; 9's complement; 10's complement; Quantum cost; Garbage output.

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1. Introduction

Quantum computing, with its notable attributes of low power consumption and high-speed operations,^[1-6] holds significant promise in the field of engineering and technology. For the high-speed computing quantum computing must be a promising field. A key component of quantum computing is reversible logic gates, characterized by an equal number of input and output terminals. In Fig. 1, we can observe the fundamental $R \times R$ reversible gate, featuring an input array (I0, I1, I2 ... IR) and an output array (O0, O1, O2, ... OR), where R is the number of input and output terminals of reversible gates. When designing and implementing reversible circuits, the critical factors to consider include delay, QC, CI, and GO.^[7-15] In the realm of reversible logic design and development, the primary goal is to minimize QC, GO, CI, and

delay. Various logic circuits, such as code converters, comparators, adders, subtractors, and multipliers, play essential roles in computing systems.^[16-23] Researchers have devoted their efforts to creating reversible combinational logic circuits. However, the development of reversible 9's and 10's complement code converters is still an area with room for improvement. The 9's complement of a decimal number is obtained by subtracting each digit from 9 and The 10's complement of a decimal number is obtained by adding 1 to the 9's complement of that number. Both the complement technique are essential for code conversion technique. Notably, Mohammadi *et al.*^[24] introduced the 9's complement code converter. This research paper presents an innovative approach, unveiling an optimized reversible 9's complement code converter and a novel 10's complement code converter. The primary focus is on minimizing delay, quantum cost, and the generation of garbage outputs.

2. Basic concepts

The core principle underlying reversible circuits involves crafting digital circuits in such a way that they can perform computations while preserving all information. Reversible circuits find applications in diverse fields, including quantum computing, cryptography, the development of energy-efficient

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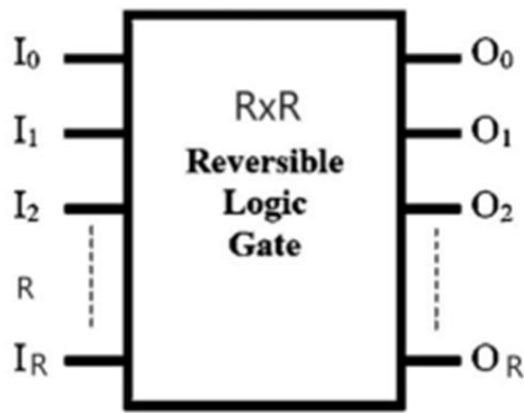


Fig. 1: $R \times R$ Reversible gate.

circuits, and certain specialized computational tasks where safeguarding data and conserving energy are of utmost importance. They provide a foundational framework for understanding the theoretical boundaries of computation and information processing.

In this research paper, we introduce a novel, cost-optimized approach for creating 9's and 10's complement code converters using quantum logic gates. There exist several types of reversible gates, which encompass the Peres gate,^[7] Feynman gate,^[6] NOT gate,^[1] controlled V gate,^[8,15] and Hadamard or H gate.^[20] However, in this study, our circuits are exclusively designed using the Peres gate (PG), Feynman gate (FG), and reversible NOT gates. While numerous authors have previously delved into reversible circuit designs such as comparators, adders, subtractors, various sequential circuits, multipliers, and dividers, there has been a lack of focus on 10's complement code converter designs. The proposed work is expected to hold significant value for the future of reversible computing. Fig. 2 - 5 provide functional representations of the controlled V gate,^[8,15] FG, NOT gate,^[1] and Peres gate.^[7]

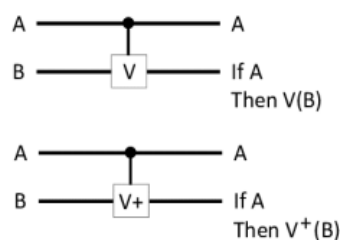


Fig. 2: 2x2 Controlled V Gates with A, B Input.

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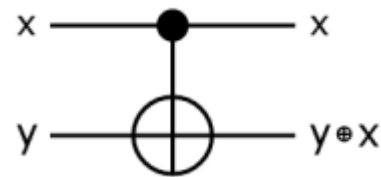


Fig. 3: 2x2 Feynman gate with x, y Input.



Fig. 4: 1x1 Reversible NOT Gate with x Input.

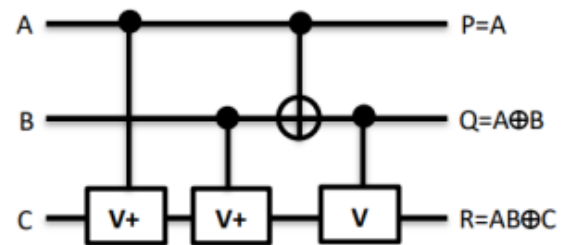


Fig. 5: 3x3 Peres Gate's Quantum representation with A, B, C Input.

3. Proposed works

In this article, the cost optimized reversible 9's complement has been proposed and also proposed the novel 10's complement code converter using basic reversible gates, such as PG, FG and NOT gates.

3.1 Proposed optimized reversible 9's Complement code converter

Fig. 6 shows the proposed cost optimized 9's complement code converter designed using PG and reversible NOT gates. The input terminals are B0 to B3 and output terminals are C0 to C3. Table 1 represents the truth table of BCD to 9's complement code.

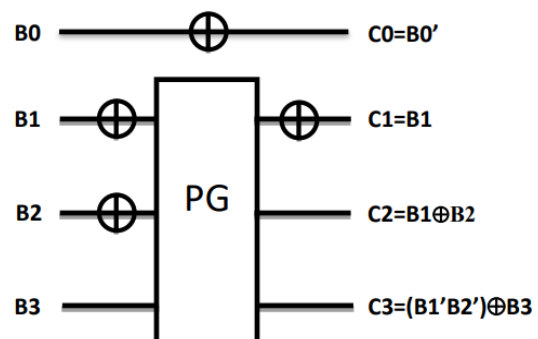


Fig. 6: Proposed 9's Complement CC using PG and NOT with QC=8, CI=0 and GO=0.

The simplified Boolean equations, as presented in Table 1, are evaluated and can be found in Eq. (1)-(4). The proposed circuit is designed using one Peres gate (PG) and

Table 1: The truth table of 9's complement code.

BCD Code				9'S Complement Code			
B3	B2	B1	B0	C3	C2	C1	C0
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0

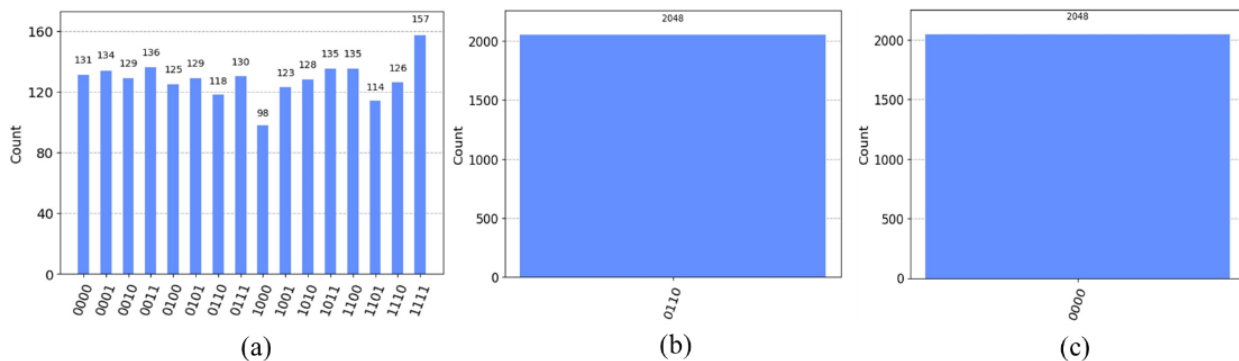


Fig. 7: (a) Verified output functions of new reversible 9's Complement using IBM Qiskit. (a) Probability function for all outputs. (b) Represents the output probability function when input is “0011”. (c) Represent the output probability function of the 9's complement of the input “1001”.

four reversible NOT gates. The quality of computation (QC) is 8, there are no garbage outputs (GO), combinational inputs (CI) total to 0, and the delay is 1. In comparison to previously reported results, there is a substantial improvement in QC, GO, CI, and Delay, with enhancements ranging from 61.9% to 73.3%, 100%, 100%, and 40% to 50%, respectively. Fig. 7(a) to 7(c) depict the output probability functions. Fig. 7(a) illustrates the probability function for all possible outputs. Fig. 7(b) represents the output probability function for the output “0110” which is the 9's complement of “0011”, Fig. 7(c) portrays the probability function of the 9's complement of the input “1001” which is “0000

$$C0=B0 \quad (1)$$

$$C1=B1 \quad (2)$$

$$C2=B1 \oplus B2 \quad (3)$$

$$C3=(B1+B2) \odot B3 \quad (4)$$

3.2 Proposed novel reversible 10's Complement code converter

In Fig. 8, we present a novel 10's complement code converter, which has been designed using Peres gates (PG), Feynman gates (FG), and reversible NOT gates. The input terminals are labeled as B0 to B3, and the output terminals are labeled as D0 to D3. The truth table for the conversion of Binary Coded Decimal (BCD) to 10's complement code is illustrated in Table 2. From Table 2, we derive the simplified Boolean equations, which are expressed as Eq. (5)-(8).

$$D0=B0 \quad (5)$$

$$D1=B0 \odot B1 \quad (6)$$

$$D2=B0B1 \oplus B2 \quad (7)$$

$$D3=(B0B1+B2) \odot B3 \quad (8)$$

The circuit for this proposal is constructed using two PGs, one FG, and three reversible NOT gates. In terms of performance

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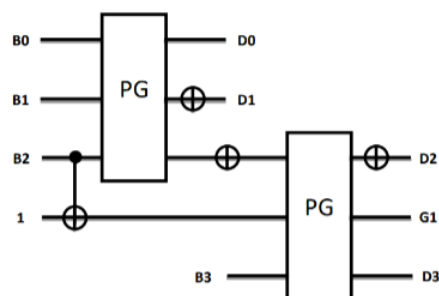


Fig. 8: Proposed new reversible 10's complement CC using PG, FG, and NOT with QC=12, CI=1, and GO=1.

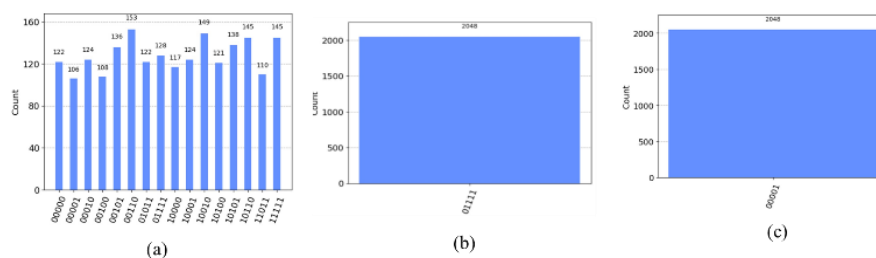


Fig. 9: (a) Verified output functions of new reversible 10's Complement using IBM Qiskit. (a) Probability function for all outputs. (b) and (c) Output probability function when input 0011 and 1001.

Table 2: Truth table of 10's complement code.

BCD Code				10'S Complement Code			
B3	B2	B1	B0	D3	D2	D1	D0
0	0	0	0	1	0	1	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	0	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	1	0
1	0	0	1	0	0	0	1

Table 3: Comparison results of 9's complement code converter.

	QC	GO	CI	Delay
Proposed work	8	0	0	3
Ref.[24]	21	1	1	5
Circuit-(a)				
Ref.[24]	30	4	4	6
Circuit (b)				
Improvement %	61.9– 73.3	100	100	40 - 50

metrics, the quality of computation (QC) is 12, there is one garbage output (GO), the number of combinational inputs (CI) is one, and the delay is four. Fig. 9(a) depicts the probability distribution for all potential outputs, while Fig. 9(b) displays the output probability functions specifically for the input “0011”. Furthermore, Fig.9(c) represents the probability

distribution for the output “0000” which is the 9's complement of “1001”.

4. Conclusion

Within this research paper, the authors introduce a new concept-a reversible 10's complement code converter-utilizing

fundamental reversible logic gates, including Peres gate (PG), Feynman gate (FG), and NOT gate. Additionally, a cost-optimized reversible 9's complement code converter is proposed, designed with the employment of PG and NOT gate. To validate these circuit designs, rigorous testing is conducted using the IBM Qiskit simulator. For the 10's complement code converter, the quantified metrics are as follows: Quality of Computation (QC) is measured as 12, Combinational Inputs (CI) total 1, there is one Garbage Output (GO), and the Delay is 4. Similarly, for the 9's complement code converter, the metrics are QC 8, CI 0, GO 0, and Delay 1. A comparison of these results is summarized in Table 3. The proposed 9's complement code converter demonstrates notable improvements, with enhancements ranging from 61.9% to 73.3% in QC, a 100% reduction in GO and CI, and a 40% to 50% decrease in delay when compared to previously reported results.^[25] This innovative design has broader applications spanning various domains, including quantum cryptography and reversible arithmetic logic units (ALU), among others.

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Conflict of Interest

There is no conflict of interest in any concern.

Supporting Information

Not applicable.

Credit Statement

Parna Kundu: Conceptualization, Literature review, Simulation work done; **Mousam Chatterjee:** Analysis, and Writing draft manuscript; **Susmita Biswas:** Analysis and Writing draft manuscript; **Himadri Sekhar Das:** Supervision, Analysis, and Writing draft, Result analysis, Editing and Correspond the final manuscript; **Gaurav Sharma:** Result analysis and Drafting; **Maitrayee Chakrabarty:** Simulation and Referencing; **Sudipta Banerjee:** Result Analysis and Plagiarism report; **Aritra Bhowmik:** Prepared figure; **Milan Hait:** Prepared the references and results; **Subir Kumar Maity:** Analysis, and Writing draft manuscript; **Heranmoy Maity:** Supervision, Conceptualization, Literature review, Correspond the paper.

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