



Design and Development of Cost Optimized Quantum Binary-Coded Decimal Adder using Reversible Logic Gates

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Abstract

Within this paper, the authors introduce a new cost optimized quantum Binary-Coded Decimal (BCD) adder circuit that utilizes reversible gates as its building blocks. The newly proposed quantum BCD adder is specifically constructed with the inclusion of double Peres gates (DPG), Peres gates (PG), BJN gates, Feynman gates (FG), and reversible NOT gates. To bring this idea to life, we undertook the design and implementation of the proposed circuit using the Qiskit simulator provided by the IBM Quantum Computing lab. Our evaluation of the newly optimized BCD adder circuit yielded the following metrics, the quantum cost of 47, the constant input of 8, garbage output of 12, and a delay of 10. When compared to previously reported results, we observed significant improvements in various aspects, with a 25.39% reduction in quantum cost, a 28.57% decrease in constant input, and a 36.84% reduction in garbage output.

Keywords: Reversible logic gate, Quantum circuit, BCD Adder, Quantum cost, Garbage output.

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1. Introduction

Quantum computing^[1-8] is highly promising in the realm of engineering and technology due to its remarkable traits, including low power consumption and high-speed operation, as evidenced in citations.^[9] Reversible logic gates are distinctive in that they feature an equal number of I/O terminals, as illustrated in Fig. 1. This depiction shows the essential $M \times M$ configuration of a reversible gate, comprising an input array (I0, I1, I2 ...IM) and an output array (O0, O1, O2, OM). In the context of designing and implementing reversible circuits, the critical parameters to consider encompass delay, quantum cost (QC), garbage output (GO), and constant input (CI), as indicated in references.^[10-17]

Within the domain of reversible logic design and development, the primary aim is to minimize delay, GO, and

QC. Researchers have dedicated substantial efforts to creating reversible combinational logic circuits, such as its complement code converters, BCD-to- Excess-3 code converters, adders, subtractors, and multipliers.^[5-9,18-19] However, its essential to highlight the limited attention given to the development of reversible BCD adder using reversible gates. The available literature features numerous instances of reversible BCD adder, as underscored in references.^[20-25]

2. Basic concepts and relevant work

The fundamental concept behind a reversible circuit^[26-30] involves the design of digital circuits in a manner that enables them to execute computations while retaining all information. Within the realm of a reversible circuit:

- (i) Information Preservation: Every input is associated with a unique output, and vice versa. Consequently, during the computation, no data is lost, and it can theoretically be reversed to recover the original inputs from the outputs.
- (ii) No Energy Loss: Reversible circuits are engineered to ideally avoid energy dissipation, including the generation of heat or any other form of energy loss. This stands in contrast to classical irreversible circuits, where energy dissipates as heat, particularly when bits are erased (e.g., in AND or OR gates).
- (iii) Input-Output Balance: In a reversible circuit, the count of input bits precisely matches the count of output bits.

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- (iv) **Deterministic Operations:** Reversible gates execute operations in a deterministic manner, without involving probabilistic actions commonly seen in quantum computing.
- (v) **Quantum Computing Relevance:** Reversible circuits hold immense significance in quantum computing. Quantum gates, by nature, are reversible due to the preservation of quantum information. Quantum computers employ reversible operations to manipulate quantum states.
- (vi) **Low Power Utilization:** Reversible circuits offer appeal in specific low-power applications since they minimize energy dissipation.

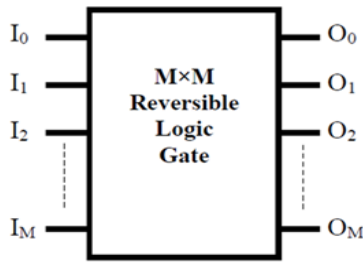


Fig. 1: M×M Reversible gate.

Reversible circuits find applications in diverse fields such as quantum computing, cryptography, the creation of energy-efficient circuits, and specific computational tasks with a focus on information security and energy conservation. They play a fundamental role in understanding the theoretical limits of computation and information processing.^[31-38]

In this paper, a new cost-optimized BCD adder design is constructed using fundamental reversible logic gates. These gates include the double Peres gate (DPG)[10], Peres gate (PG)[10], BJN gate[25], reversible NOT gate[2], and Feynman gate(FG)[6]. The QC of DPG, PG, BJN, NOT and FG gates are 6, 4, 5, 1 and 1 respectively. Block diagram and quantum realization of PG, DPG, FG, BJN and NOT shown in Fig. 2(a) to Fig. 6. While various authors have previously proposed reversible BCD adder designs, our work stands out for its significant cost-efficiency improvement of approximately 25.39%. The distinct characteristic of our proposed reversible adder approach adds significant value to its suitability for quantum computations. In Fig. 7 and Fig. 8, the complete adder is depicted utilizing DPG, while the half adder design employs PG.

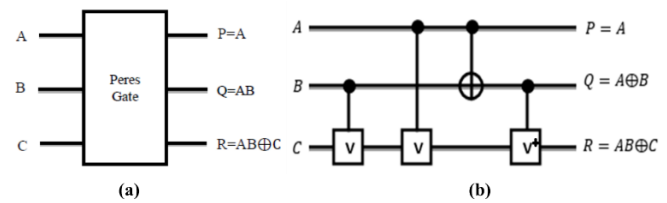


Fig. 2: (a) Block diagram of PG. (b) Quantum realization of PG.

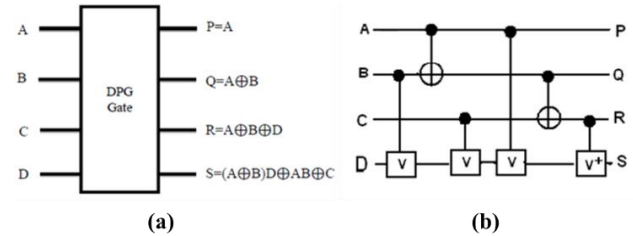


Fig. 3: (a) Basic block diagram of DPG. (b) Quantum realization of DPG.

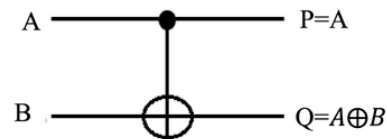


Fig. 4: Quantum realization of FG.

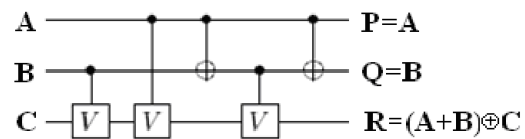


Fig. 5: Quantum realization of BJN.



Fig. 6: Quantum realization of NOT.

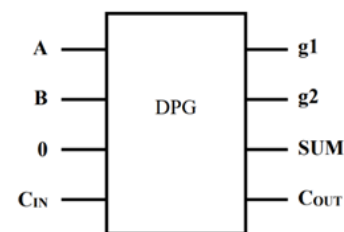


Fig. 7: Full adder using DPG with QC=6, CI=1, GO=2.

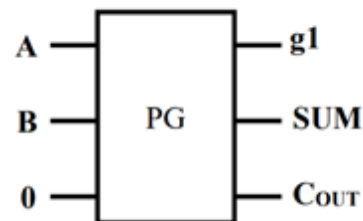


Fig. 8: Half adder using PG with QC=4, CI=1, GO=1.

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3. Proposed quantum reversible BCD adder

In this article, the process of designing a BCD adder entails the combination of two BCD numbers to yield a BCD sum, ensuring that the outcome conforms to BCD conventions, where no digit exceeds 9 (1001 in binary). To execute binary addition within the BCD adder, Full Adders are employed as a fundamental component. The design of the Full Adder in this paper involves the use of DPG gates, with each Full Adder incurring a quantum cost of 6. Specifically, the implementation involves eight DPG gates, as well as one BJN

gate and one PG gate, accompanied by three FG gates and two NOT gates.

Furthermore, the design encompasses a BCD correction circuit, for which one BJN gate, one PG gate, three FG gates, and two NOT gates are utilized. Ultimately, the corrected 4-qubit BCD sum stands as the definitive output of the BCD adder. Fig. 9 shows the 1st design of proposed circuit using eight full adders with QC 62. Fig. 10 shown the simplified proposed circuit using four full adder and two half adder with 47 QC.

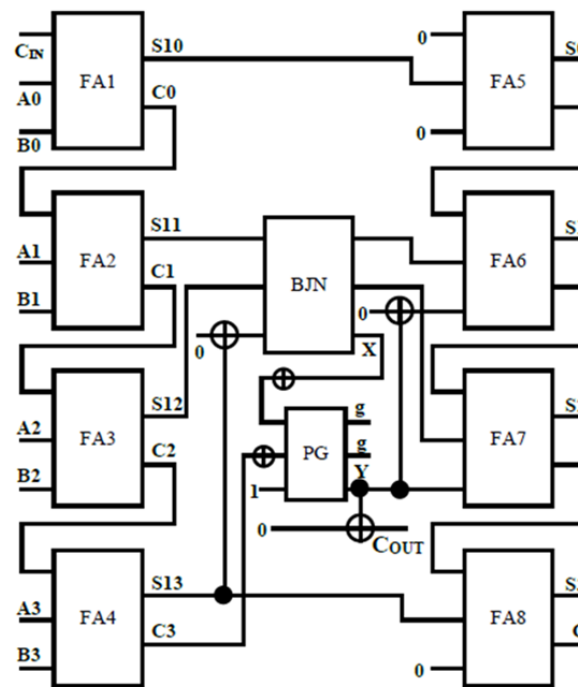


Fig. 9: Design-1: BCD Adder using eight full adder with QC 62.

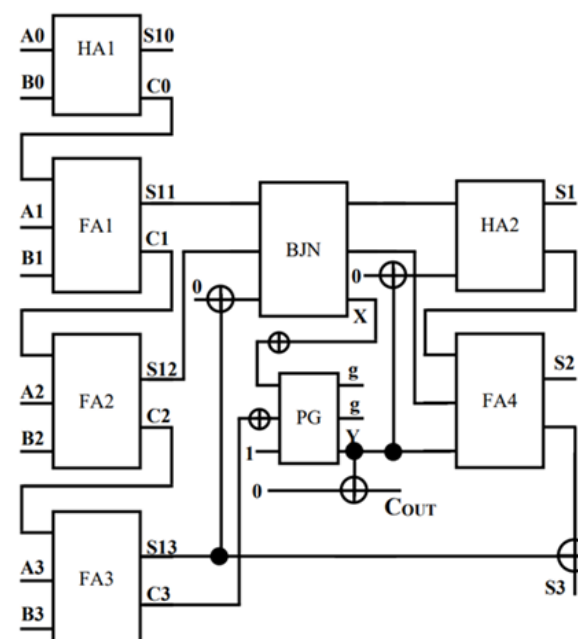


Fig. 10: Design-2: BCD adder four full adder and two half adder with QC 47.

Table 1: Comparison results.

	QC	CI	GO	Delay	Ref.
Proposed design	47	10	12	10	
2020	63	14	19	10	[20]
2015	113	13	24	-	[21]
2012	90	19	24	-	[22]
2011	70	1	5	57	[23]
2008	81	17	22	-	[24]
2007	99	7	11	-	[25]
2006	137	12	22	-	[26]
2005	157	17	22	-	[27]
Improvement % w.r.t previous reported result	25.39 %	28.57 %	36.84 %	0 %	

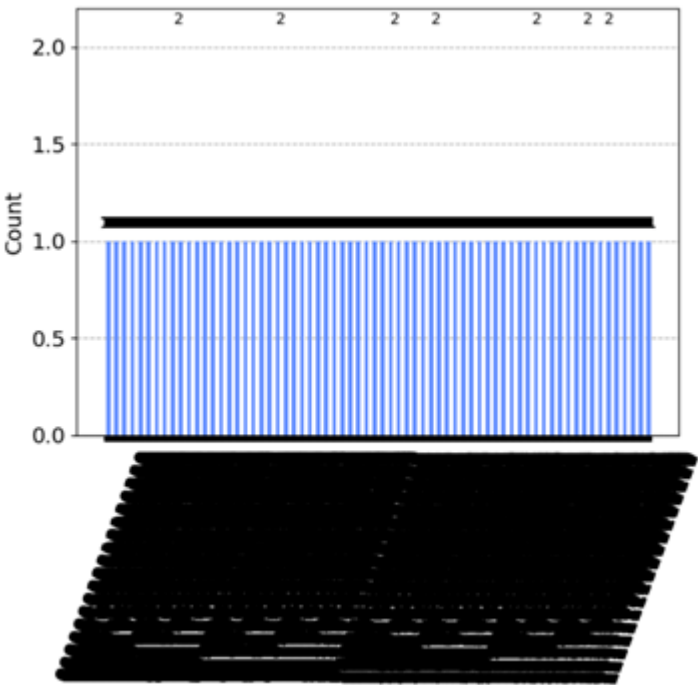


Fig. 11: 18 Qubit (For 8 BCD input and 10 constant input) output function.

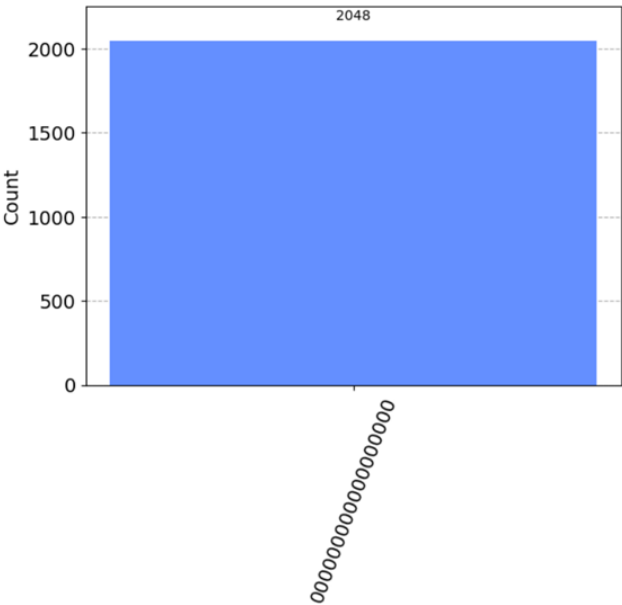


Fig. 12: Output probability function for the output ‘000000000000000000’.

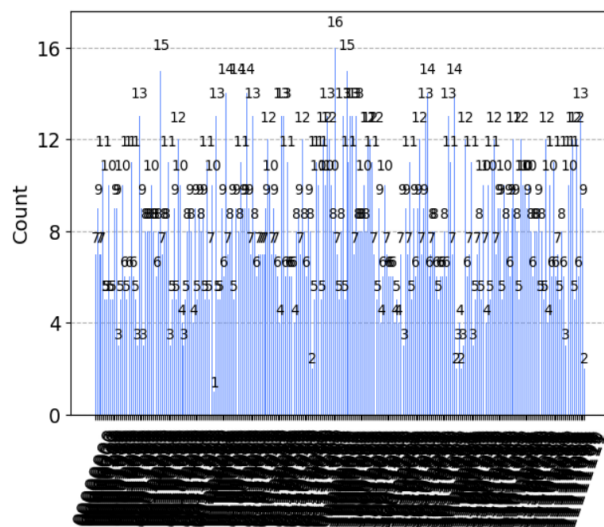


Fig. 13: Output probability function of the 8 Qubit BCD correction circuit.

4. Results analysis of the proposed work

In this paper, the authors present a new approach: a cost-efficient reversible BCD adder created with reversible gates. The quantum cost of this innovative quantum BCD adder is calculated as 47. It has a constant input of 8 and a garbage output of 12. In comparison, the garbage output for a full reversible adder using DPG is 2, while a half adder using PG has a garbage output of 1. The design incorporates four reversible full adders, two reversible half adders, and two garbage outputs from the control circuit, which uses PG, BJN, and FG. These results demonstrate a significant advancement over previously reported findings from 2020 [20], with improvements of 25.39%, 28.57%, and 36.84% in garbage output, respectively. Table 1 presents a comparison of these results. The proposed design is validated using the IBM Qiskit simulator, an open-source software toolkit for quantum computing. Qiskit facilitates the development and management of quantum programs and allows execution on either IBM Quantum Platform's prototype devices or local simulators.

Fig. 11 illustrates the simulation of 18 qubits for basic circuit verification, with a total of 18 input terminals. Among these, 4 are qubit two Binary-Coded Decimal (BCD) inputs, and there is a total of 10 constant inputs. Within the 10 constant inputs, 4 come from the BCD correction circuit, 4 from the first 4-qubit adder, and 2 from the second 4-qubit adder. The delay of the proposed circuit is 10, because maximum propagation quantum gates are 10. The BCD correction circuit receives 4 inputs from the first 4-qubit adder and 4 constant inputs. In Fig. 12, the probability function for the single output '0000000000000000' is depicted, and similar probability functions can be derived for all other outputs. Fig. 13 displays the probability function for the 8-qubit reversible BCD correction circuit within the proposed circuit. It's important to note that all simulations were conducted solely for circuit validations

5. Conclusion

In this paper, the authors present a new quantum BCD adder circuit that is designed and implemented using reversible gates. The quantum cost (QC), control inputs (CI), gate operations (GO), and delay for this newly developed circuit are measured as 47, 8, 12, and 10, respectively. In comparison to previously reported outcomes, this innovative design demonstrates substantial improvements w.r.t. previously reported results in 2020[20], boasting a 25.39% reduction in quantum cost, a 28.57% decrease in constant input, and a 36.84% reduction in garbage outputs. The proposed design is applicable to a range of fields, including quantum computing, cryptography, and reversible arithmetic logic units (ALUs), among others.

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Conflict of Interest

There is no conflict of interest.

Supporting Information

Not applicable.

CRedit Statement

Parna Kundu: Conceptualization, Literature review, Simulation work done. **Mousom Chatterjee:** Analysis, and writing draft Manuscript. **Susmita Biswas:** Analysis and writing draft Manuscript. **Himadri Sekhar Das:** Supervision, analysis, and Writing draft, result analysis, editing and correspond the final manuscript. **Santanu Mishra:** Result analysis and drafting. **Swarnajit Bhattacharya:** Simulation and referencing. **Sudipta Banerjee:** Result analysis and plagiarism report. **Aritra Bhowmik:** Prepared figure. **Heranmoy Maity:** Supervision, Conceptualization, literature review, correspond the paper.

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