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Distributed Generator Offset Armored Synchronous Reference Frame-Phase-Locked Loop using Arbitrary Delay Signal Cancellation for Grid Connected Modular Multilevel Converter

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Abstract

This paper addresses the distributed generator (DC) offset problem in the grid-connected modular multilevel converter and proposes a simple solution adopting a three-phase synchronous reference frame (SRF) phase-locked loop (PLL) and an arbitrary delay signal cancellation (ADSC). The ADSC is used to mitigate DC offset, along with phase and amplitude correction methods, to accurately estimate the grid voltage's phase, frequency, and amplitude. The proposed method is not limited to a specific delay time, unlike the other PLLs. This freedom in selecting the delay time can be used to enhance the dynamic response of the grid synchronization unit, which is essential for MCC's power flow. The small-signal model of the proposed PLL is derived, which paves the way to study its closed-loop stability and provides guidelines to design the loop filter gains. Simulation results demonstrate the viability of the proposed PLL when used with the grid-connected 5-level Modular Multilevel Converter (MMC) system. Compared with the αβDSC-PLL, the proposed method reduces total harmonic distortion (THD) by up to 70% and improves DC voltage settling time by more than 50%, confirming its practical viability and robustness.

Keywords: Phase-locked loop; Modular multilevel converter; Grid synchronization; Small-signal analysis.
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1. Introduction

The rise in global energy demand and growing awareness of global warming have opened the door to connecting renewable energy sources to the grid.[1-3] This is done using grid synchronized power electronics converters. Grid synchronization is the process of estimating the grid frequency, phase, and voltage amplitude.[4] Synchronization techniques are employed to achieve fast, accurate grid synchronization between the converter and the grid. The phase-locked loop (PLL) is a common method for grid synchronization in distributed generator (DG) systems.[5-7] One of the most popular PLLs is based on a synchronous reference frame (SRF), from which many other PLLs have originated.[8-10] Fig. 1 shows the SRF-PLL block diagram. The first stage of this PLL is the Phase Detector (PD), generating an error signal proportional to the phase difference between the input and the reference. Loop Filter (LF) comes after to estimate the frequency of the electrical grid. The last stage of this controller is the Voltage Control Oscillator (VCO), which provides the estimated phase.

In Fig. 1, $v_{\alpha\beta}$ is the $\alpha\beta$-axis voltage, v_q is q-axis voltage, ω_n is nominal grid frequency, $\hat{\omega}_g$ is the estimated grid frequency, and $\hat{\delta}$ is the estimated grid phase. The grid voltage v_{abc} is transformed into dq reference frame utilizing Clarke's and Park's transformations in the PD part, using $\hat{\omega}_g$. The dq voltage contains the phase error and amplitude information of the grid voltage. Without loss of generality, v_q is assumed to be the controllable part of the signal that is regulated employing the LF as shown in Fig. 1. The LF usually is a proportional integrator (PI) controller. The LF output is processed through the VCO to estimate the grid phase.

Although the SRF-PLL is effective at estimating the grid information under normal conditions, it exhibits sinusoidal

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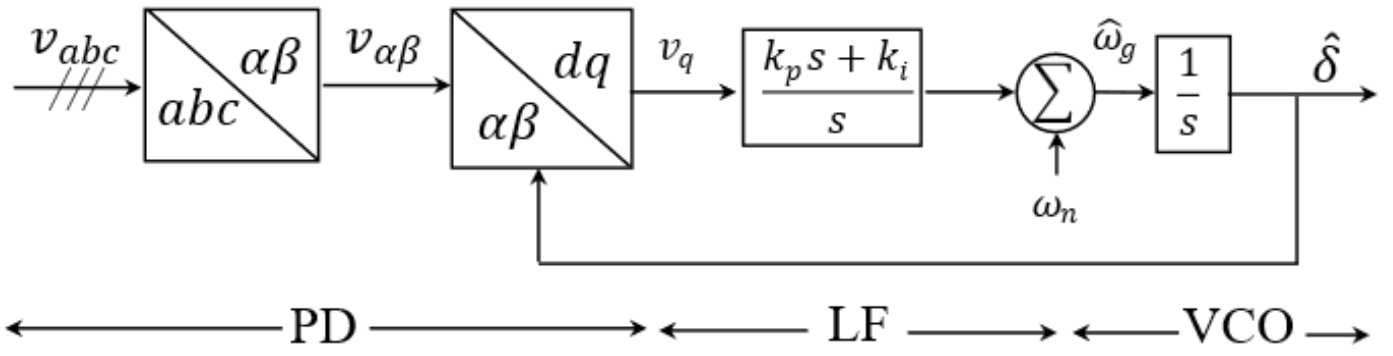

Fig. 1: Synchronous Reference Frame PLL.

ripples in the estimated electrical grid frequency, phase, and voltage amplitude under abnormal conditions such as harmonics and DC offset.[11,12] The existence of the DC offset may be related to measurement device offsets, the use of analogue-to-digital (A/D) converters, the implementation of control algorithms on embedded platforms, and grid faults.[13-15]

The operation of the grid synchronization unit is a critical component in the performance of Modular Multilevel Converters (MMCs) utilized in modern grid-connected applications.[16] Its precise functionality is essential for ensuring the effective exchange of active and reactive power, minimizing circulating currents, and maintaining balanced sub-module capacitor voltages.[17] The overall stability of the MMC depends on accurate, timely measurements of the grid voltage's phase, frequency, and amplitude. Inadequate synchronization may pose significant risks, including degraded power quality, conservative control strategies, and the unwarranted activation of protection mechanisms.[18] These challenges can severely impact power-flow control in MMCs, particularly in High Voltage Direct Current (HVDC) systems, expansive photovoltaic (PV) arrays, and sophisticated energy storage solutions. A common practical challenge is DC offset in the sensed grid signals: even small DC components produce erroneous projections that the PLL interprets as phase error, leading to steady or oscillatory phase/frequency estimation errors, injected distortion, and degraded DC-link voltage dynamics in the MMC. Because MMC control relies on accurate phase/frequency for circulating current suppression and capacitor balancing, an unmitigated DC offset can directly impair power flow control, increasing THD and settling times.[19] Therefore, many PLLs have been proposed in the literature to mitigate the influence of DC offset on grid synchronization.[20-24]

The αβ Delayed Signal Cancellation (αβDSC) operator, combined with the SRF-PLL, is used for DC-offset mitigation with a phase-error compensator in.[16,17] The counterpart of this PLL uses the dqDSC in the inner-loop filter.[22,23] Although DSC-based PLLs can mitigate DC offset, their dynamic response exhibits slow transients. A modified dqDSC is proposed in [24] to accelerate the conventional dqDCS PLL. However, the PLL's performance degrades under frequency drift; therefore, to regain performance, the DSC block must be adaptive, which complicates PLL analysis and loop filter design.

In,[25] a DC-immune PLL (DCI-PLL) is proposed for DC-offset rejection in the synchronous reference frame. The DCI-PLL was robust and efficient, but its disadvantage is that the algorithm is computationally expensive due to the use of the cotangent function. In the outer loop, an adaptive low pass filter is adopted for DC offset mitigation in[26] showing good DC rejection capability. However, the adaptation path in the outer loop complicates the PLL analysis and loop filter design.

In this paper, a simple DC-offset rejection-based SRF-PLL is proposed for three-phase grid synchronization. Mathematical derivations and a small single model are derived for the proposed PLL, facilitating the study of its closed-loop stability and providing guidelines for specifying the loop filter gains based on the given requirements. Moreover, the proposed method is not limited to a specific delay time, unlike the other PLLs. This freedom in selecting the delay time can enhance the synchronization unit's dynamic response.

Simulation results show that the proposed PLL is effective in the grid-connected 5-level Modular Multilevel Converter (MMC) system. Compared to the αβDSC-PLL, the proposed method reduces total harmonic distortion (THD) by up to 70% and shortens DC bus voltage settling time by over 50%, confirming its practical usability and robustness.

2. The proposed PLL

In the presence of the DC-offsets, the grid voltage is given by

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega_g t + \theta) \\ \sin\left(\omega_g t + \theta - \frac{2\pi}{3}\right) \\ \sin\left(\omega_g t + \theta + \frac{2\pi}{3}\right) \end{bmatrix} + \begin{bmatrix} V_a^{DC} \\ V_b^{DC} \\ V_c^{DC} \end{bmatrix} \quad (1)$$

where V_m is the grid voltage amplitude, ω_g is the grid frequency, and θ is the initial phase angle. V_a^{DC}, V_b^{DC}, and V_c^{DC} are the DC-offset components. Using a coordinate transformation, the grid voltage v_{abc} is transformed into a stationary reference frame as in Eq. (2)

$$v_{\alpha\beta} = T_{\alpha\beta}^{abc} v_{abc} \quad (2)$$

Where $T_{\alpha\beta}^{abc}$ can be defined as shown in Eq. (3),

$$T_{\alpha\beta}^{abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (3)$$

Eq. (2) can be rewritten as in Eq. (4)

$$v_{\alpha\beta}(t) = v'_{\alpha\beta}(t) + V_{\alpha\beta}^{DC} \quad (4)$$

in which $v'_{\alpha\beta}(t)$ is defined in Eq. (5)

$$\begin{bmatrix} v'_\alpha(t) \\ v'_\beta(t) \end{bmatrix} = \sqrt{\frac{3}{2}} V_m \begin{bmatrix} \sin(\delta) \\ -\cos(\delta) \end{bmatrix} \quad (5)$$

where $\delta = \omega_g t + \theta$ is the grid phase, and the DC component can be written as

$$\begin{bmatrix} V_\alpha^{DC} \\ V_\beta^{DC} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} V_a^{DC} - \frac{1}{2} V_b^{DC} - \frac{1}{2} V_c^{DC} \\ \frac{\sqrt{3}}{2} V_b^{DC} - \frac{\sqrt{3}}{2} V_c^{DC} \end{bmatrix} \quad (6)$$

The signal in Eq. (6) is passed through an ADSC as shown in Fig. 2, delaying the signal using a delay operator of τ seconds, yields Eq. (7).

$$\begin{bmatrix} v_\alpha(t-\tau) \\ v_\beta(t-\tau) \end{bmatrix} = \sqrt{\frac{3}{2}} V_m \begin{bmatrix} \sin(\delta - \omega_g \tau) \\ -\cos(\delta - \omega_g \tau) \end{bmatrix} + \begin{bmatrix} V_\alpha^{DC} \\ V_\beta^{DC} \end{bmatrix} \quad (7)$$

To this end, the output of the DSC block can be written in Eq. (8) as

$$\Delta v_{\alpha\beta} = v_{\alpha\beta}(t) - v_{\alpha\beta}(t-\tau) \quad (8)$$

which can be written as

$$\begin{bmatrix} \Delta v_\alpha \\ \Delta v_\beta \end{bmatrix} = \begin{bmatrix} v'_\alpha(t) \\ v'_\beta(t) \end{bmatrix} - \begin{bmatrix} \cos(\omega_g \tau) & \sin(\omega_g \tau) \\ -\sin(\omega_g \tau) & \cos(\omega_g \tau) \end{bmatrix} \begin{bmatrix} v'_\alpha(t) \\ v'_\beta(t) \end{bmatrix} \quad (9)$$

Define a transformation matrix T as in Eq. (10)

$$T(\omega_g \tau) = \begin{bmatrix} \cos(\omega_g \tau) & \sin(\omega_g \tau) \\ -\sin(\omega_g \tau) & \cos(\omega_g \tau) \end{bmatrix} \quad (10)$$

then, Eq. (9) can be written in Eq. (11) as

$$\Delta v_{\alpha\beta} = \left(I_{2\times 2} - T(\omega_g \tau)\right) v'_{\alpha\beta} \quad (11)$$

Integrating the DSC block into the SRF-PLL rejects the DC offset. However, phase and voltage-magnitude scaling are introduced due to the use of the DSC block. Therefore, phase

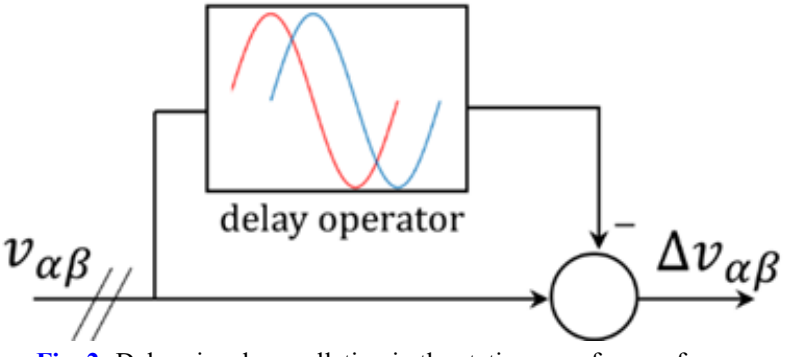

Fig. 2: Delay signal cancellation in the stationary reference frame.

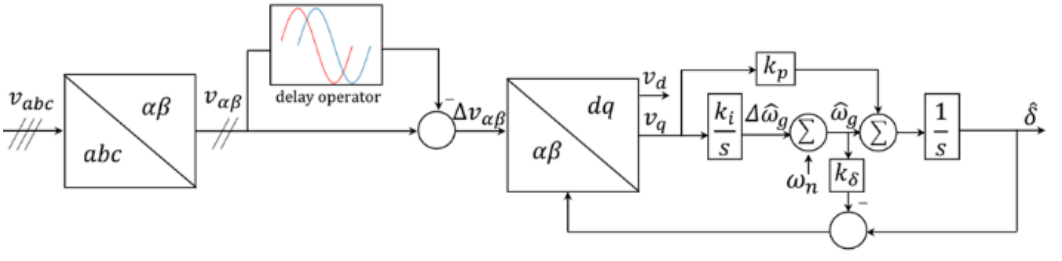

Fig. 3: The proposed PLL utilizes an arbitrary time delay block.

and voltage amplitude correction methods are also proposed in this paper, as shown in Fig. 3.

The signal in dq-reference frame as a function of phase correction δ_0 can be written as:

$$v_{dq} = \left[T(\delta + \delta_0) - T\left(\delta + \delta_0 + \omega_g \tau\right)\right] v'_{\alpha\beta} \tag{12}$$

Setting $\delta_0 = -\frac{\omega_g \tau}{2}$ in Eq. (12), yields

$$v_{dq} = \left[T\left(\delta - \frac{\omega_g \tau}{2}\right) - T\left(\delta + \frac{\omega_g \tau}{2}\right)\right] v'_{\alpha\beta} = T(\delta)\left[T^t\left(\frac{\omega_g \tau}{2}\right) - T\left(\frac{\omega_g \tau}{2}\right)\right] v'_{\alpha\beta} \tag{13}$$

where, T^t is the matrix transpose. Simplifying the terms inside the bracket yields

$$T^t\left(\frac{\omega_g \tau}{2}\right) - T\left(\frac{\omega_g \tau}{2}\right) = 2\sin\frac{\omega_g \tau}{2}\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix} \tag{14}$$

Substituting Eq. (14) into Eq. (13) yields

$$\begin{bmatrix}v_d\\ v_q\end{bmatrix} = 2\sin\left(\frac{\omega_g \tau}{2}\right) T(\delta)\begin{bmatrix}-v'_\beta\\ v'_\alpha\end{bmatrix} \tag{15}$$

Substituting Eq. (1) into Eq. (15) and simplifying, yields

$$\begin{bmatrix}v_d\\ v_q\end{bmatrix} = \sqrt{6}\sin\left(\frac{\omega_g \tau}{2}\right)\begin{bmatrix}V_m\\ 0\end{bmatrix} \tag{16}$$

From Eq. (16), v_d contains information about the voltage amplitude, while v_q contains information about the grid phase. Therefore, the utilized DSC operator adds a phase that is equal to $\frac{\omega_g \tau}{2}$ and scales the voltage amplitude by $k_a = \sqrt{6}\sin\left(\frac{\omega_g \tau}{2}\right)$.

3. The small-signal model of the proposed PLL

From Fig. 3, the following can be deduced:

$$v_{dq} = \left[T\left(\hat{\delta} - \frac{\hat{\omega}_g \tau}{2}\right) - T\left(\hat{\delta} - \frac{\hat{\omega}_g \tau}{2} + \omega_g \tau\right)\right] v'_{\alpha\beta} \tag{17}$$

where, $\delta = \delta_n + \Delta\delta$, $\hat{\delta} = \delta_n + \Delta\hat{\delta}$, $\omega_g = \omega_n + \Delta\omega_g$, and $\hat{\omega}_g = \omega_n + \Delta\hat{\omega}_g$, $\hat{\delta}$ is the estimated phase and $\hat{\omega}_g$ is the estimated grid frequency.

Eq. (17) is written as:

$$v_{dq} = \left[T\left(\hat{\delta} - \frac{\omega_n \tau}{2} - \frac{\Delta\hat{\omega}_g \tau}{2}\right) - T\left(\hat{\delta} - \frac{\omega_n \tau}{2} + \omega_g \tau - \frac{\Delta\hat{\omega}_g \tau}{2}\right)\right] v'_{\alpha\beta} \tag{18}$$

The use of the grid estimated information would disturb the synchronization process. Therefore, a stabilizing controller should be designed to maintain v_q at zero position. This can be done using the small-signal model to design a proportional-integral (PI) controller.

Near synchronization, the following relations hold: $\sin^2\left(\frac{\Delta\omega_g \tau}{2}\right) \approx 0$, $\cos^2\left(\frac{\Delta\omega_g \tau}{2}\right) \approx 1$, $\sin\left(-\frac{\Delta\hat{\omega}_g \tau}{2}\right) \approx -\frac{\Delta\hat{\omega}_g \tau}{2}$, and $\cos\left(-\frac{\Delta\hat{\omega}_g \tau}{2}\right) \approx 1$. Therefore, Eq. (18) is simplified by adopting the Taylor series expansion and ignoring the high-order terms yields Eq. (19)

$$v_q \approx \sqrt{\frac{3}{2}} V_m \left\{2\sin\left(\frac{\omega_n \tau}{2}\right)\left(\Delta\delta - \Delta\hat{\delta}\right) + 2\sin\left(\frac{\omega_n \tau}{2}\right)\frac{\Delta\hat{\omega}_g \tau}{2} - \sin\left(\frac{\omega_n \tau}{2}\right)\Delta\omega_g \tau\right\} \tag{19}$$

which simplified to

$$v_q \approx \sqrt{6} V_m \sin\left(\frac{\omega_n \tau}{2}\right)\left\{\left(\Delta\delta - \Delta\hat{\delta}\right) + \frac{\Delta\hat{\omega}_g \tau}{2} - \frac{\Delta\omega_g \tau}{2}\right\} \tag{20}$$

Let $K_\delta = \sqrt{6} V sin\left(\frac{\omega_n \tau}{2}\right)$, then Eq. (20) is rewritten as:

$$v_q \approx K_\delta\left[\frac{\Delta\delta + \Delta\delta - \Delta\omega_g \tau}{2} - \Delta\hat{\delta} + \frac{\Delta\hat{\omega}_g \tau}{2}\right] \tag{21}$$

The Laplace transform of Eq. (21) is

$$v_q(s) \approx K_\delta\left[\frac{1 + e^{-\tau s}}{2}\Delta\delta(s) - \Delta\hat{\delta}(s) + \frac{\Delta\hat{\omega}_g(s)\tau}{2}\right] \tag{22}$$

The small-signal model is plotted in Fig. 4 with the help of Fig. 3 and Eq. (22) where $k_\delta = \frac{\tau}{2}$ represents the phase correction gain. From Fig. 4, the closed-loop transfer function is constructed as:

$$G(s) = \frac{\Delta\hat{\delta}}{\Delta\delta} = \frac{1 + e^{-\tau s}}{2}\frac{k_\delta\left(k_p s + k_i\right)}{s^2 + k_\delta\left(\left(k_p - k_i\tau/2\right)s + k_i\right)} \tag{23}$$

Eq. (23) describes a second-order system whose characteristic equation is $s^2 + k_\delta\left(k_p - k_i\tau/2\right)s + k_\delta k_i = 0$, k_δ is a constant depending on the adopted delay operator. Therefore, without loss of generality, it can be assumed that $k_\delta > 0$. Thus, for Eq. (23) for stability, the following conditions in Eq. (24) must be satisfied:

$$k_p > k_i\tau/2 \text{ and } k_i > 0 \tag{24}$$

The time response characteristic of the time-invariant second-order system is related to its natural frequency (ω_0) and damping ratio (ξ). Therefore, if ω_0 and ξ are given, the controller gains are determined as shown in Eq. (25):

$$k_i = {\omega_0}^2 \quad \text{and } k_p = \frac{2\xi\omega_0}{k_\delta} + k_i\tau/2 \tag{25}$$

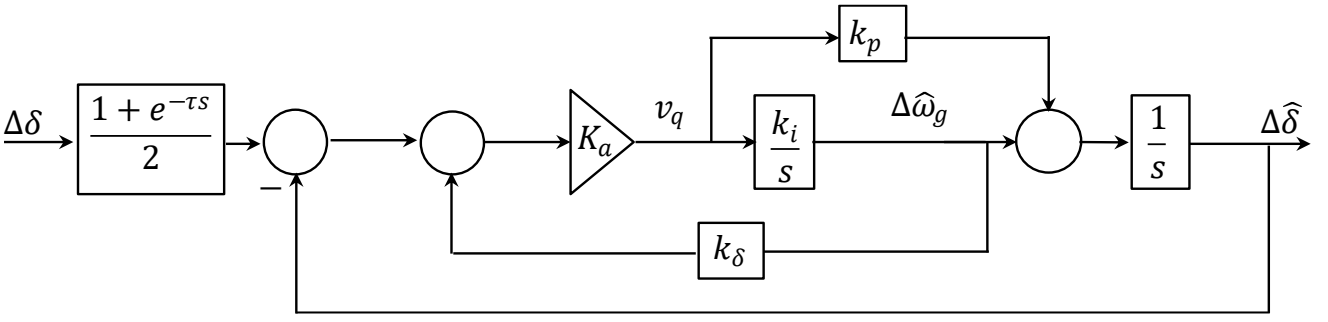

Fig. 4: The small signal mode of the proposed PLL.

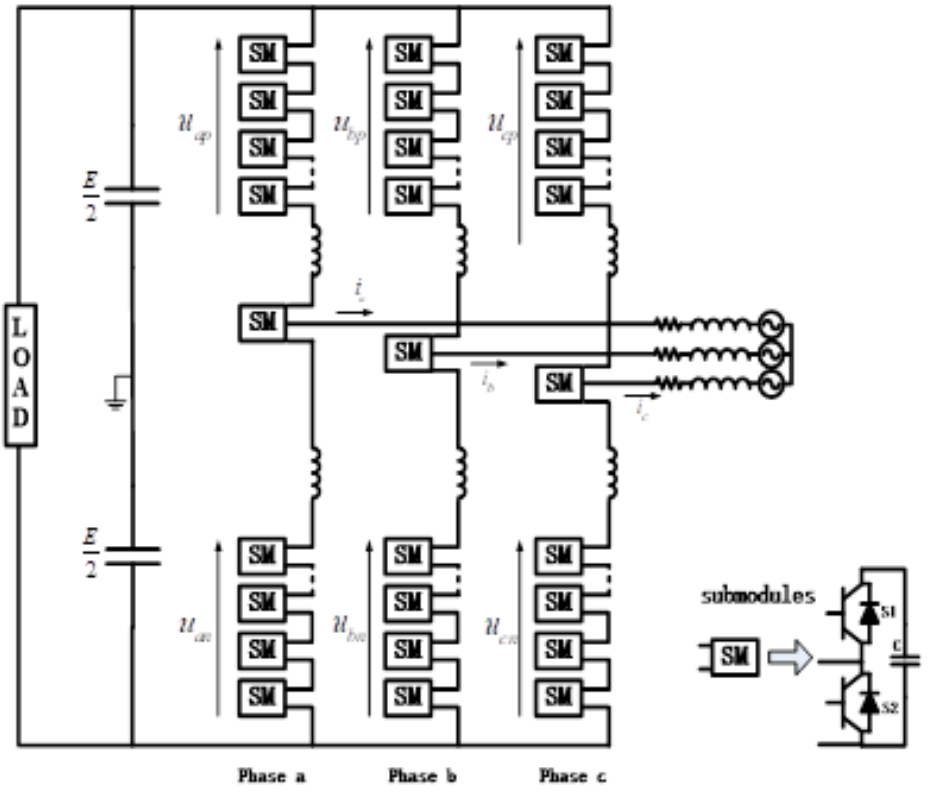

Fig. 5: 5-levels MMC connected to the grid. The standard submodule connections are used to achieve the 5-level output.

4. Simulation verification

To validate the proposed PLL, it will be used in a practical system to study its effect on DC-offset rejection and grid current and voltage synchronization using MATLAB/Simulink. The system consists of five levels of MMC (5L-MMC) connected to the electrical grid as shown in Fig. 5, 5L-MMC is a bidirectional converter connected to three phase voltages from the AC input/output side to get DC voltage from the output/input side, each AC phase voltage is connected to one leg, and the leg consists of upper arm and lower arm. Each arm has four submodules to produce four voltage levels, in addition to the zero level; the total number of levels on the ac voltage side is five. The choice to use MMC is because the trend worldwide is to use high-voltage DC (HVDC) systems to transfer electrical power from one country to another, or from remote areas such as offshore wind farms to the load. One of the best choices is to use MMC to convert the transferred DC power to grid power.

Field-Oriented Control (FOC) is selected for MMC closed loop control because it provides precise, decoupled regulation of the dq-axis currents, enabling accurate active and reactive power control with minimal cross-coupling. By operating in the synchronous reference frame, FOC improves dynamic response, enhances stability, and simplifies current-loop tuning despite the MMC's complex internal dynamics. It also effectively suppresses circulating currents and harmonics, resulting in lower distortion and improved power quality. These capabilities make FOC a robust and efficient control strategy for grid-connected MMC applications. However, without accurate grid information, FOC cannot operate accurately.

The DC voltage side serves as the reference for the outer

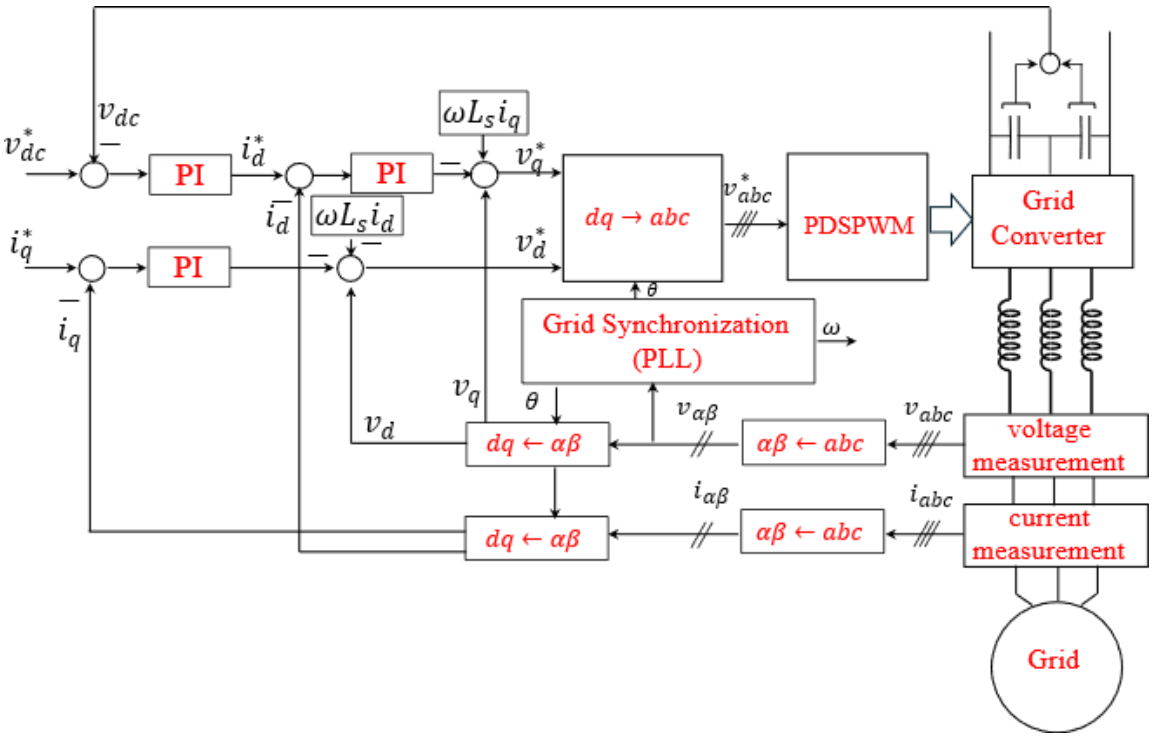

Fig. 6: MMC control model.

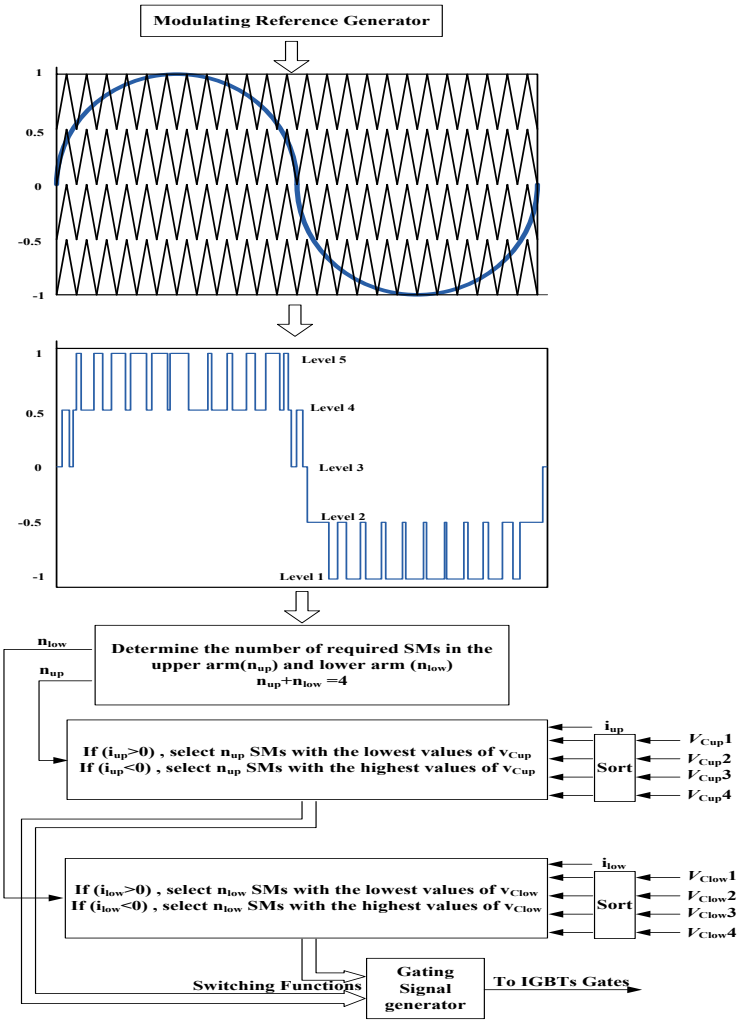

Fig. 7: PDPWM method for MMC.

Table 1: The system and control parameters.

No.	Parameter	Value
	MMC parameters	
1	Input line voltage	25kVrms
2	Output voltage	33kV DC
3	Grid frequency	50 Hz
4	No. submodules per arm	4
5	Submodule capacitor	2700 μF
6	Arm inductor	3e-3 H
7	Arm resistor	1 Ω
8	Filter inductor	3e-3 H
9	Filter resistor	0.05 Ω
10	DC side capacitor	7500 μF
	Proposed PLL parameters	
11	kp	568
12	ki	50473
13	ka	1
14	τ	0.002
15	kδ	τ/2

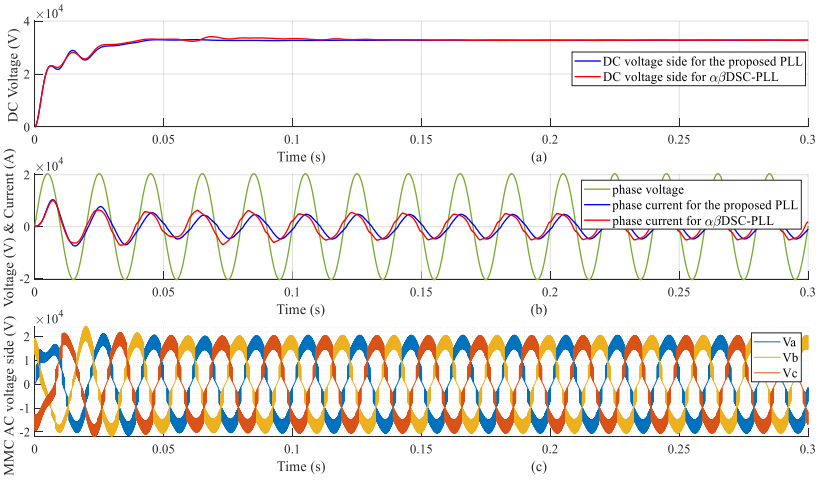

Fig. 8: System performance at normal operation. (a) is the MMC DC voltage side. (b) is the grid voltage and current. (c) is the MMC AC voltage side.

loop, which controls the PI controller; the outer loop's output is used as a reference for the inner loop, which the PI controller also controls to regulate the current components id and iq as shown in Fig. 6. The output of the FOC is used as a reference for the phase disposition sinusoidal PWM (PDSPWM). The procedure of PDSPWM used in MMC for balancing the capacitor is shown in Fig. 7,[27] and the system and proposed PLL parameters are shown in Table 1.

The system is numerically simulated to study system performance when the proposed PLL is used, compared with the αβDSC-PLL, under various transient and grid disturbance conditions. Under normal operation, the performance of the proposed PLL and the αβDSC-PLL is shown in Fig. 8. From the results, the DC voltage settled to within 0.05s around twice the grid cycle using the proposed PLL, with a phase shift between the grid voltage and current close to zero. In contrast, the system needed five grid cycles to settle down when using the αβDSC-PLL. Moreover, a phase shift between the grid voltage and current is observed.

A 10% third and fifth harmonics are injected into the grid from 0.4s to 0.6s to assess the system's performance. When the proposed PLL is used with the system, the DC voltage returns to its final value immediately after the harmonics are removed. In contrast, when using αβDSC-PLL, the DC voltage required nearly 0.1s to reach the final value, with considerable overshoot. The DC offset of the current started at 0.4 for five cycles is 0.69%, with a phase shift between the grid voltage and current close to zero, even under harmonic injection, as shown in Fig. 9.

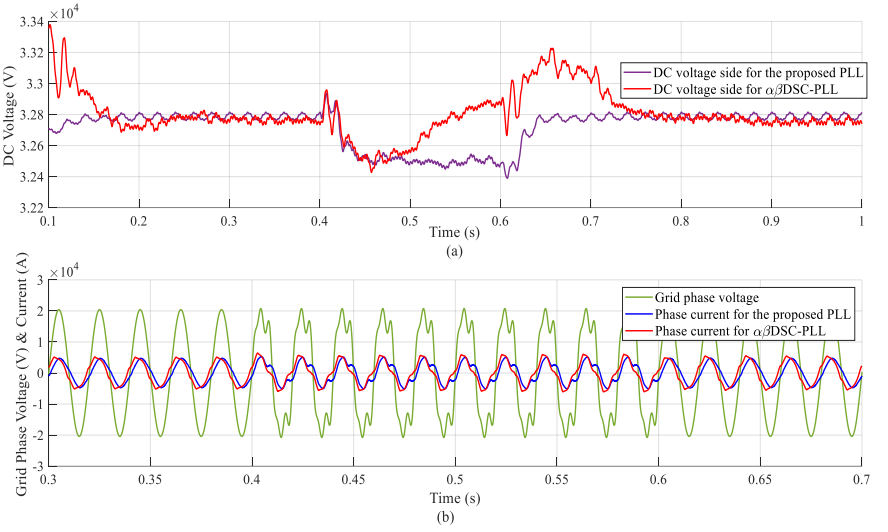

Fig. 9: System performance when harmonics are injected to the grid. (a) MMC DC voltage side. (b) grid voltage and current.

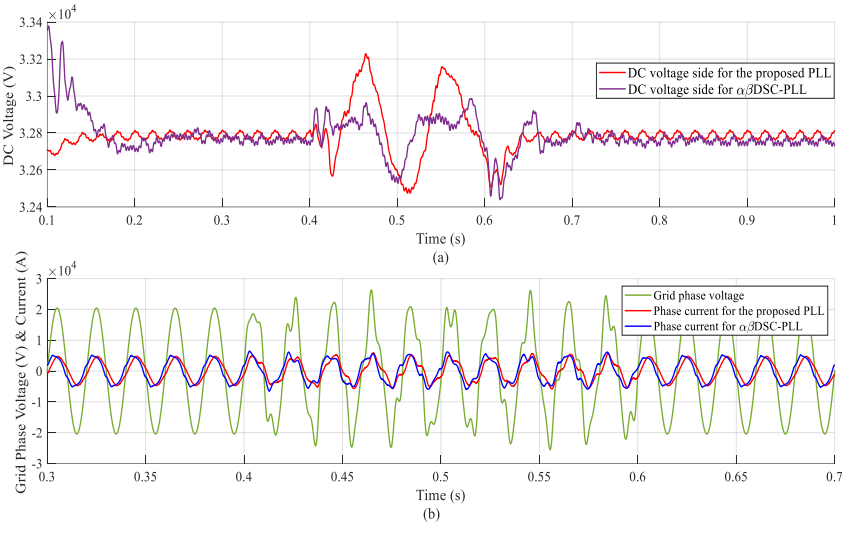

Fig. 10: System performance when interharmonics are injected into the grid. (a) is the MMC DC voltage side. (b) is the grid voltage and current.

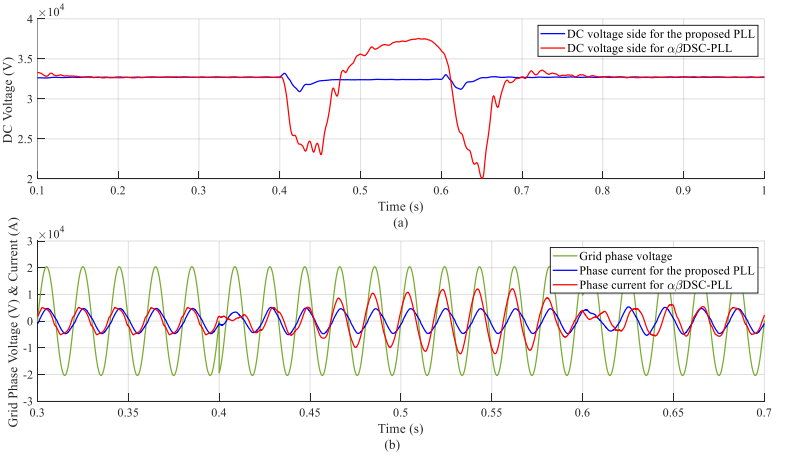

Fig. 11: System performance when overfrequency. (a) is the MMC DC voltage side. (b) is the grid voltage.

Another distortion occurs on the grid; 3.2th and 4.7th harmonics are injected into the grid from 0.4s to 0.6s. These were chosen to test the robustness of the proposed PLL against non-characteristic frequencies that standard fixed-filter PLLs might struggle to reject. The DC voltage oscillation in the transient response when using the proposed PLL is much better than with the αβDSC-PLL. The DC offset of the current, which started at 0.4, remains at 0.57% for five cycles, with a phase shift between the grid voltage and current close to zero, even under interharmonic injection. The current shape is better during the distortion period, adopting the proposed PLL, as shown in Fig. 10.

When the grid frequency is raised from 50Hz to 52Hz over 0.4s to 0.6s, as shown in Fig. 11, the system exhibits excellent performance with the proposed PLL, and the DC voltage changes little during the over-frequency disturbance. A large change in DC voltage with high overshoot occurs when the αβDSC-PLL is used with the system. Moreover, the magnitude of the grid current remains unchanged when over-frequency is applied using the proposed PLL. An apparent change in grid current magnitude is observed when the αβDSC-PLL is used with the system.

When under-frequency is applied to the systems, the frequency is reduced to 48.5Hz. The DC voltage drops significantly, and the magnitude of the grid current increases when using an αβDSC-PLL, as shown in Fig. 12. In contrast, using the proposed PLL, the DC voltage exhibits a stable response and recovers faster than the αβDSC-PLL. The DC offset of the grid current starts at 0.4s for five cycles under overfrequency and underfrequency conditions, adopting the proposed PLL, are 1.83% and 4.5%, respectively, compared to 6.35% and 6.83% when the αβDSC-PLL is used.

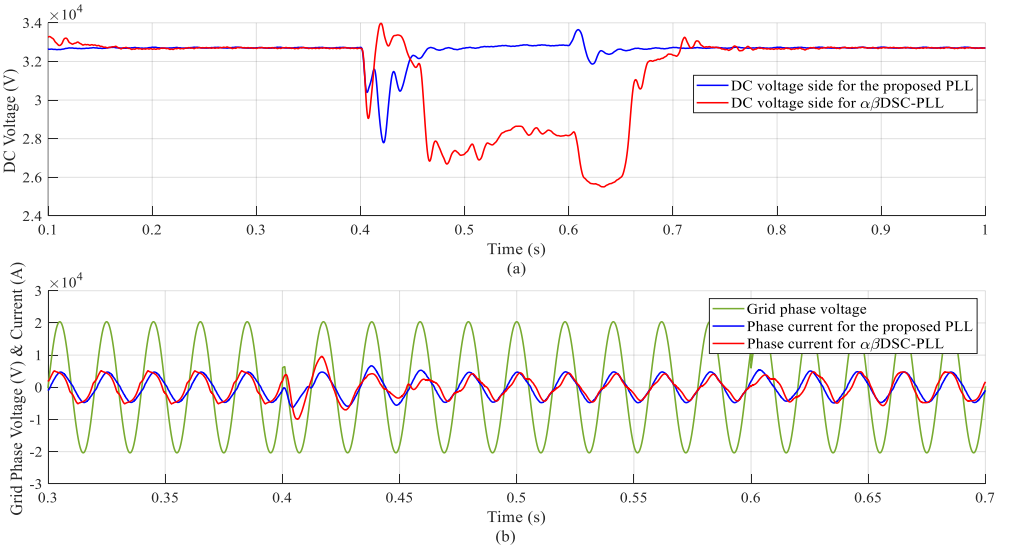

Fig. 12: System performance when underfrequency. (a) is the MMC DC voltage side. (b) is grid voltage.

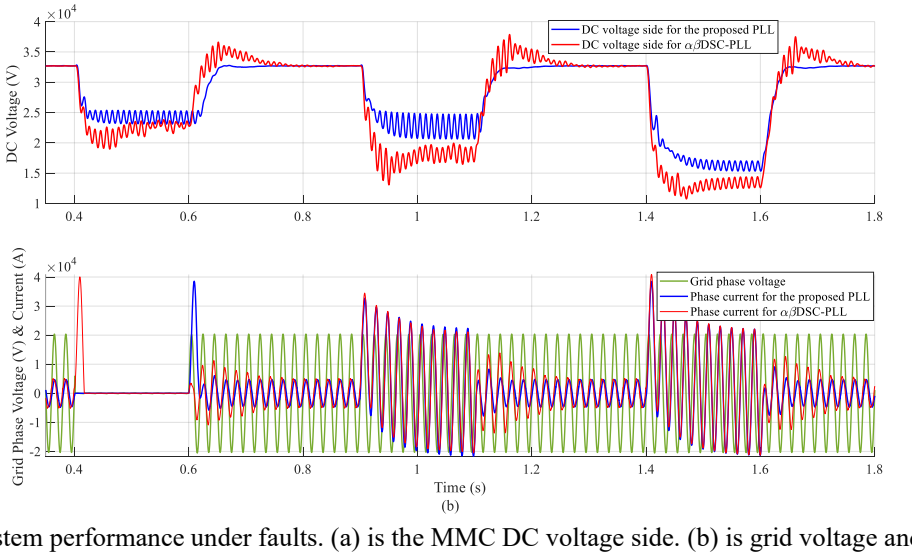

Fig. 13: System performance under faults. (a) is the MMC DC voltage side. (b) is grid voltage and current.

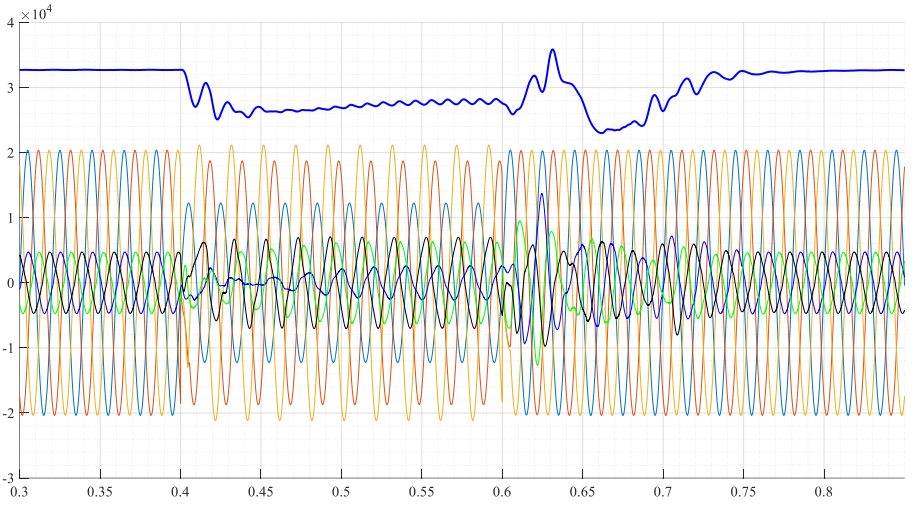

Fig. 14: Grid phase voltages and currents, and DC voltage side when the proposed PLL is used.

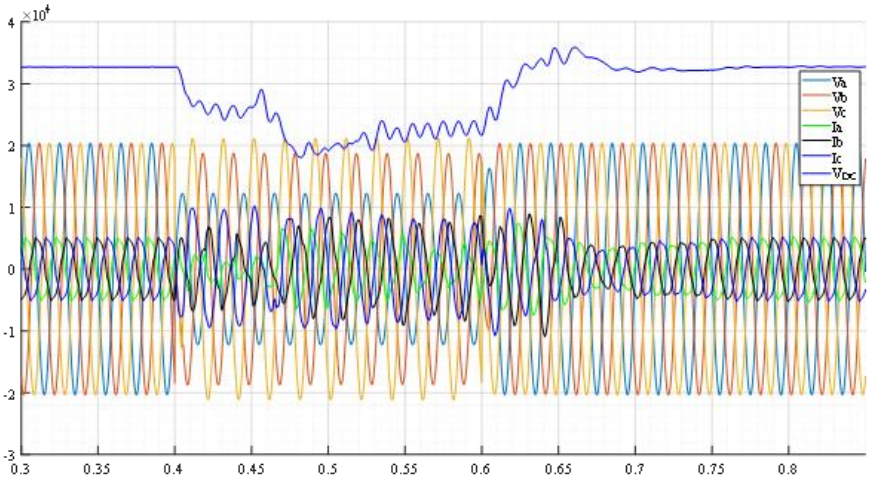

Fig. 15: Grid phase voltages and currents, and DC voltage side when αβDSC PLL is used.

The system is subjected to various faults: a single-phase-to-ground fault from 0.4s to 0.6s, a two-phase fault from 0.9s to 1.1s, and a two-phase-to-ground fault from 1.4s to 1.6s. With the proposed PLL, the change in DC voltage during fault periods is smaller, and it returns to its final value immediately upon fault removal. Moreover, the shape of the grid current is better, especially after the faults are removed. However, when using αβDSC-PLL with the system, the DC voltage after each fault took longer to settle to its final value. This means that the system's performance under various faults is much better with the proposed PLL, as shown in Fig. 13.

If the grid is subjected to unbalanced voltages so that grid phase voltages become 21kV, 18.5kV, and 12kV instead of 20kV at normal operation, and the unbalanced voltages are applied between 0.4 and 0.6 seconds. From Figs. 14 and 15, it can be seen that the DC voltage shape on the MMC DC side is much better when the proposed PLL is used than with the αβDSC-PLL. Moreover, it can be seen that the currents under αβDSC-PLL is higher and distorted than in the case of the proposed PLL.

5. Conclusion

This work presents an accurate and simple phase-locked loop for grid synchronization in modular multilevel converters by integrating a synchronous reference-frame PLL with an arbitrary-delay signal cancellation block. This method effectively suppresses DC offset and ensures accurate estimation of the grid information needed for modular multi-level converter operation. Additionally, the flexibility in delay selection significantly improves dynamic performance. The derived small-signal model offers valuable insights into stability studies and facilitates systematic controller design.

Simulation results confirm the effectiveness of the proposed approach, demonstrating notable improvements in total harmonic distortion and DC voltage settling time compared to $\alpha\beta$DSC phase-locked loop. These findings indicate that the ADSC-enhanced SRF-PLL is a practical, robust, and efficient solution for grid-connected MMC applications.

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Conflict of Interest
There is no conflict of interest.

Supporting Information
Not applicable.

CRediT Statement
Firas A. Obeidat: Conceptualisation, Methodology, Investigation, Formal analysis, Data curation, Software, Validation, Writing – Original draft, Writing – Review & editing. **Issam A. Smadi:** Conceptualization, Methodology, Investigation, Software, Writing – Review & editing. **Saher Albatran:** Conceptualisation, Writing – Review & editing. **Mohammad Bany Issa:** Conceptualisation, Methodology, Softwware, Writing – Original draft.

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